

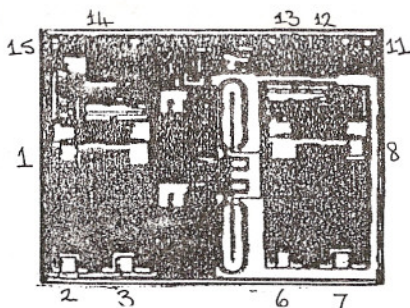


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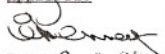
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Chip Dimensions (mils.): 160 x 120 x 20	Bond Pads: 4 x 4 min.
HARRIS HIP25001	Issue 1

Pad	Function	Pad	Function	NOTES:
1	LO	9	NC	Functions are as the 16 pin DIP and SOIC packages.
2	COM	10	NC	
3	V _{CC}	11	V _{DD}	NC = No Connect
4	NC	12	HIN	
5	NC	13	SD	
6	V _s	14	LIN	
7	V _s	15	V _{DD}	
8	HO	16	NC	

E & O E. The supply of dice to this layout can only be guaranteed if it forms part of a specification or the chip identification, if below, is requested. Chip back potential is the level at which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated above. If no potential is given the chip back should be isolated. Nominal metallisation thicknesses are based on manufacturer's information. Tolerance on chip dimensions +/-3 mils.

Approved: 	Metallisation/Thickness(KA) Top : Al Back: Si	Chip Identification Line Source: Mask Ref : 45010 Process : Version : Geometry :
Date: 2-9-99	Back Potential: Man's. Part No:	

Topside Metal: Al

Backside: Si

Backside Potential:

Mask Ref: 45010

Bond Pads : .004 min

APPROVED BY: CB

MFG: Harris

DIE SIZE: .160" x .120"

THICKNESS: .020"

DATE: 2/6/01

P/N: HIP-2500-6